Amendments to the Specification:

On page 4, please delete paragraph 0017.

On page 4, please amend paragraph 0018 as follows:

FIGURE ~~5~~ **4** is a top plan view of an alternate embodiment for the semiconductor package of the present invention; and

On page 4, please amend paragraph 0019 as follows:

FIGURE ~~6~~ **5** is a side elevation cross-section view of the semiconductor package of FIGURE ~~5~~ **4** taken along line 6-6.

On page 4, please amend paragraph 0020 as follows:

Referring first to FIGS. 1 through 3, a semiconductor package 10 is shown construed in accordance with the principals of the present invention. The semiconductor package 10 includes a semiconductor chip 20 having an upper surface 30, a perimeter 40 and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70 is disposed on the upper surface 30 of the semiconductor chip 20. A chip paddle 80 having a top surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a perimeter 140 ~~(Fig. 4)~~ and a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

On page 4, please amend paragraph 0021 as follows:

Referring now to FIGS. 1 through ~~-4-~~ **3** in combination, a leadframe 170 is shown having a plurality of tie bars 180, a side surface 190 and a bottom surface (not shown). The tie bars 180 are connected to the corners 130 of the chip paddle 80. The tie bars 180 externally extend from the chip paddle 80. The leadframe 170 further has a plurality of dam bars 220.

On page 5, please amend paragraph 0023 as follows:

Referring to FIG. 2, there is disclosed a ground ring 262 formed in the half-etched section 150 of the chip paddle 80. The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230. The ground ring 262 may be interchangeably used as a power ring should circumstances require. The upper surface 264

of the ground ring 262 is planar with the upper surface **90** of the chip paddle 80 and the upper surface ~~236~~ **235** of the leads 230.

On page 5, please amend paragraph 0027 as follows:

Referring now to **FIG. 4 and** FIG. 5, an alternate embodiment for a semiconductor package 11 is shown. In this embodiment, the chip paddle 80 is provided with a plurality of tabs 310 in the half-etched section 150 of the chip paddle 80 for the similar purpose of increased bonding strength. It is also contemplated that the combination of through holes 300 (Fig. 1) and tabs 310 may be used to increase the bonding strength of the encapsulation material 280 in the package 10.

On page 6, please amend paragraph 0028 as follows:

The tabs 310 are formed in the half-etched section 150 of the chip paddle 80. The tabs 310 must extend to a limited degree to prevent a short circuit forming between the tabs 310 and the leads 230. It is preferable that the number of the tabs 310 corresponds to the number of the grounding input bond pads 60 and output bond pads 70 of the semiconductor chip 20. The tabs 310 may be formed by chemical etching when patterning the entire leadframe ~~170~~ **171** and also by other mechanical methods depending on the requirements of the individual package11. By increasing the area or length of the chip paddle 80, the tabs 310 are easily bonded with conductive wires 270 by increasing the area for which to connect the conductive wires 270. The tabs 310 may serve to function as a ground or power ring in certain applications. It is to be noted that the hatched areas in FIG. ~~5~~ **4** are the half-etched sections of the paddle 80 and leads 230.

On page 6, please amend paragraph 0029 as follows:

~~Referring now to FIG. 6, a cross-sectional view of the semiconductor package 11 taken along line 6-6 of FIG. 5 is shown.~~ The tab 310 is electrically connected to the semiconductor chip 20 via conductive wire 270.